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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/032,168	12/21/2001	Aaron Wallack	C01-001	6052

23459 7590 11/09/2004

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EXAMINER	
STREGE, JOHN B	
ART UNIT	**PAPER NUMBER**
2625	

DATE MAILED: 11/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/032,168	WALLACK, AARON	
	Examiner	Art Unit	
	John B Strege	2625	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-2,8-17,22-27,33-37* is/are rejected.

7)☒ Claim(s) *3-7,18-21 and 28-32* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/2/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-2,8,11,15-17,22,25,27, and 33-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gallarda et al. USPN 6,539,106 (hereinafter "Gallarda").

Claim 1 discloses, "an image data analysis method for inspecting pads of electronic devices, the method comprising: acquiring an image corresponding to a pad." Gallarda discloses a method and apparatus for the detection of defects in patterned substrates, such as semiconductor wafers (corresponding to a pad) particularly based on features in voltage-contrast images (col. 1 lines 34-37, image is acquired as seen in step 320 of figure 3).

Claim 1 further recites, "generating binarized image data from the image." Gallarda discloses extracting feature objects by thresholding the feature image to produce a binary image (at least col. 5 lines 35-40, col. 10 lines 64-66, and col. 11 lines 5-15).

Claim 1 further recites, "generating a list of dark regions from the binarized image and selecting at least one dark region from the list of dark regions." Gallarda discloses that a list of features extracted from the image is prepared (col. 14 lines 58-62, also shown in figure 18h). As seen in the figures 19a-19g, the regions extracted are dark

regions. Gallarda recites that these features are extracted from a grayscale image (col. 14 lines 20-41), however within the cited passage does not explicitly disclose that the regions may come from a binary image as well. However it would be obvious to generate the list of features from the binarized image with the motivation that it is a conventional method used to extract features. Gallarda supports this by stating, "methods consistent with the present invention extract features from an image, such as by thresholding to produce a binary version of the feature image and then an optional grayscale image..." (col. 5 lines 35-40).

Claim 1 further recites, "generating edge data by performing edge detection on a portion of the image corresponding to the at least one dark region." Gallarda discloses that that edges of a feature in the image are detected (col. 13 lines 55-65).

Claim 1 concludes reciting, "computing a boundary description of the at least one dark region using the binarized image data and the edge data." Gallarda discloses that knowing the center point and edge of a feature, a grouping of pixels from the image which lie within the boundary of the edge are taken as defining the feature.

Regarding claim 2, Gallarda discloses that by removing the background (or masking the background) can improve the robustness of the feature extraction (col. 10 lines 38-67). Gallarda further discloses using the binary image as a mask (col. 12 lines 60-67). Gallarda also discloses that images can be aligned for mapping of the features (col. 5 lines 39-47). Gallarda does not explicitly disclose registering the pad by searching the image for a known model of the pad. However it is well known to register a pad using fiducials thus the Examiner declares official notice. It would have been

obvious to one of ordinary skill in the art to register the pad by searching for a fiducial in order to ensure accurate images of the pad areas of interest are taken.

Regarding claim 8, Gallarda discloses that properties of the features are determined such as the area (col. 7 lines 35-47, col. 14 lines 42-62).

Claim 11 has some similar limitations to claim 1 that have already been discussed such as acquiring an image, generating binarized image data from the image, generating a list of dark regions from the binarized image, and generating edge data by performing edge detection on a portion of the image. Claim 11 further recites, "applying heuristic refinement of a plurality of the dark regions using the binarized image data and the edge data to provide a set of modified regions, and merging the modified regions." Gallarda discloses using a blob analysis operation such as a computer algorithm linked_list_of_blob_features (corresponding to a heuristic refinement) that combines (merges) image regions to modify the extracted feature data (paragraph bridging col. 12 and col. 13). This can be used in combination with edge detection in the image model matching system disclosed in the paragraph bridging col. 13 and col. 14.

Claims 15 and 27 have similar limitations as claim 1, thus the same arguments used for the rejection of claim 1 apply equally to the rejection of claims 15 and 27.

Regarding claim 16, Gallarda discloses a camera (205 figure 2) and a machine vision processor coupled to the camera (figure 2 and the paragraph bridging col. 4-5).

Regarding claim 17,Gallarda discloses an algorithm for blob analysis operation linked_list_of_blob_features (corresponding to heuristic refinement) and further discloses edge enhancement (col. 11 lines 1-5).

Claims 22 and 33 are similar to claim 8, thus the same limitations used for the rejection of claim 8 apply equally to claims 22 and 33.

Claims 25 and 34 are similar to claim 11, thus the same arguments used for the rejection of claim 11 apply equally to the rejection of claims 25 and 34.

3. Claims 12-14,26, and 35-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gallarda et al. USPN 6,539,106 in view of Gonzalez et al (*Digital Image Processing,* 1993, hereinafter "Gonzalez").

In regards to claims 12 and 35, Gallarda does not explicitly disclose the edge data subsequently chained to provide edge chain data.

Gonzalez teaches chaining edge data to provide edge chain data (linking, page 429, section 7.2, first paragraph).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate Gonzalez's chaining to Gallarda's method because chaining assembles edge pixels into meaningful boundaries (Gonzalez, page 429, section 7.2 first paragraph).

Regarding claims 13-14, 26, and 36-37 Gonzalez discloses that there may be noise along the boundary (linking, page 429, section 7.2, first paragraph) thus it would be obvious to carry out heuristic refinement to remove extraneous material.

4. Claims 9-10, and 23-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gallarda et al. USPN 6,539,106 in view of Yamamoto et al. USPN

5,214,712 (hereinafter "Yamamoto") and further in view of Gonzalez et al (*Digital Image Processing,* 1993, hereinafter "Gonzalez").

As discussed above for the rejection of claim 1, Gallarda discloses acquiring an image, generating binarized image data from the image, generating a list of dark regions from the binarized image, and selecting at least one dark region in the list of dark regions. Gallarda does not explicitly disclose that the dark region has at least one distal end and pruning necks from the at least one distal end of the at least one dark region to provide a modified region. Gallarda does disclose computing a boundary description of the modified region (paragraph bridging col. 12 and col. 13, and col. 14 lines 42-62).

Yamamoto discloses a method for inspection of defects on a printed circuit board (col. 1 lines 5-10) by acquiring an image corresponding to a region of inspection (col. 2 lines 47-52); and generating binarized image data from the image (col. 2 lines 54-59). Yamamoto discloses selecting a dark region corresponding to a through hole and performing morphing using expansion and contraction to provide a modified region (col. 2 line 61 – col. 3 line 11). This allows for more accurately detecting the defects occurring on the circuit board.

Gonzalez discloses that dilation and erosion are two important morphological operations that smooth the contour of an image, breaks narrow isthmuses, and eliminates thin protusions (pg 524, first paragraph of section 8.4.2). Furthermore Gonzalez discloses that pruning methods are an essential complement of thinning and skeletonizing algorithms, because these procedures tend to leave parasitic components

that need to be cleaned up by postprocessing (page 540, first paragraph of pruning section).

Gallarda, Yamamoto, and Gonzalez are all analogous art because they are all from the same field of endeavor of image processing.

At the time of the invention it would have been obvious to one of ordinary skill in the art to combine Gallarda and Yamamoto to perform morphing to eliminate thin protrusions present with the defect image, and further combine Gonzalez to perform pruning on the defect images to eliminate extraneous materials. The motivation for doing so would be to more accurately detect defects on the circuit board. Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to combine Gallarda, Yamamoto, and Gonzalez to obtain the invention as specified in claim 9.

Regarding claim 10, Gonzalez discloses that the morphological technique using pruning starts with the assumption that the length of a parasitic component does not exceed three pixels, thus setting an elongation threshold.

Claim 23 is similar to claim 9, thus the same argument used for the rejection of claim 9 applies equally to claim 23.

Claim 24 is similar to claim 10, thus the same argument used for the rejection of claim 10 applies equally to claim 24.

Allowable Subject Matter

Claims 3-7, 18-21, and 28-32 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. USPN 6,289,126 discloses a method for determining the boundary of an object using a binary image and edge tracing.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John B Strege whose telephone number is (703) 305-8679. The examiner can normally be reached on Monday-Friday between the hours of 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bhavesh Mehta can be reached on (703) 308-5246. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JS

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